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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,134	04/03/2001	Sanjay S. Talreja	42390P9599	4900

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EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	4

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,134	TALREJA ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1-19 are represented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 04/03/2001 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2 and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin., US Patent 5,954,828.

Regarding claim 1, Lin teaches that an integrated circuit comprising:

a memory array (Fig.1, array 10), wherein the memory array is divided into m partitions is taught as array 10 in Fig.1 is divided into header section 12 and fault tolerant section which includes multiple segments (col.11, lines 60-64) , wherein m is an integer greater than or equal to two (col.11, lines 60-64);

a microcontroller (Fig.1, state machine 19 and col.5, lines 41-48) coupled to a status register (status register 38), wherein the status register reports status information of m memory partitions (col.11, lines 27-33).

Regarding claim 2, Lin teaches that the memory array is coupled to the status register by a decoder circuit (Fig.1, array 10 is couples to the status register 38 by XDEC and YDEC).

Regarding claim 18, Lin teaches that an apparatus comprising: means for partitioning a memory array (col.11, lines 60-64) to enable multiple operations to be performed on the memory array at the same time (reading, programming, erasing as

taught in col.5, lines 41-42); and means for monitoring the operations performed on the memory array (col.6, lines 44-49).

Regarding claim 19, Lin teaches that further comprising a means for communicating the status of the operations performed on the memory array to a user (Fig.1, status register coupled to the output buffer 28).

7. Claims 1-6,12-14,16 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Alexis et al., US Patent 6,182,189 B1.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Alexis teaches that an integrated circuit comprising:

a memory array (Fig.1, memory array 130), wherein the memory array is divided into m partitions (first and second planes 135 and 140), wherein m is an integer greater than or equal to two (as shown in Fig.1);

a microcontroller (col.3, lines 63-67) coupled to a status register (Fig,1, status register 150), wherein the status register reports status information of m memory partitions (col. 4, lines 3-7).

Regarding claim 2, Alexis teaches that the memory array (Fig.1, memory array 130) is coupled to the status register (Fig.1, status register 150) by a decoder circuit (X decoder and Y decoder).

Regarding claim 3, Alexis teaches that further comprising:

the microcontroller (col.3, lines 63-67) coupled to a logic block (Fig.2, RWW circuitry); the logic block coupled to the status register (as shown in Fig.2); the status register coupled to a user interface (Fig.2).

Regarding claim 4, Alexis teaches that further comprising:

the user interface coupled to an address latch (Fig.2, interface 145 coupled to read and write control circuitry); the address latch coupled to the logic block (read and write control circuitry coupled to RWW circuitry).

Regarding claim 5, Alexis teaches that the user interface communicates status register information to be used to decide subsequent operations (col.6, lines 1-8).

Regarding claim 6, Alexis teaches that a method of reading while writing to a memory array, comprising:

dividing the memory array into n planes(first and second planes 135 and 140), wherein n is an integer greater than or equal to two (as shown in Fig.1); defining a write partition, wherein the write partition is a single plane of the memory array (col.3, lines 47-50 and col.4, lines 51-65); defining a read partition, wherein the read partition is made up of all of the remaining n planes of the memory array (col.3, lines 47-50 and col.4, lines 51-65); providing the status of the read partition and the write partition of the memory array with a single status register (col.4, lines 3-7).

Regarding claim 12, Alexis teaches that a method of operating a status register, comprising: receiving a plane memory address and signals (Fig.2, address and data and control signals) from the user interface (Fig.2, interface 145) latching a plane memory address whenever a write operation is beginning or resuming (col.6, lines 52-57); evaluating the current command plane address (the command address for the write operation) with the previous plane memory address (the command address for the read operation) (col.6, lines 52-60); outputting status bits to the user interface (col.6, lines 44-50 and lines 59).

Regarding claim 13, Alexis teaches that a comparator is used to evaluate the current command plane address with the previous plane memory address (col.6, lines 52-60).

Regarding claim 14, Alexis teaches that the output status bits comprise:

a device write status bit, wherein the device write status provides the status of the block erase or program completion in the device; it is taught as the write operation has been completed as shown in col.6, lines 56-57.

a partition write status bit, wherein the partition write status provides the block erase or program executions in the current plane. It is taught as the read operation directed to the first plane as shown in col.6, lines 52-53.

Regarding claim 16, Alexis teaches that the device write status bit and the partition write status bit are not busy at the same time. It is taught as the read request can not be serviced until the write operation has been completed (col.6, lines 54-57).

Regarding claim 18, Alexis teaches that an apparatus comprising: means for partitioning a memory array (first and second planes 135 and 140 as shown in Fig.1) to enable multiple operations to be performed on the memory array at the same time (read-while-write operation); and means for monitoring the operations performed on the memory array (col.4, liens 3-7).

Regarding claim 19, Alexis teaches that further comprising a means for communicating the status of the operations performed on the memory array to a user (Fig.2, the status register coupled to the user interface 145).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexis et al., US Patent 6,182,189 B1.

Regarding claim 7, Alexis teaches the claimed invention (independent claim 6), Alexis does not teach that the memory array consists of multiple 4 Mb memory planes. Alexis only teaches the memory array including two planes and may be more than two planes and those planes include different physical memory locations in a contiguous memory array or those planes located on a different integrated circuit device (col.3, lines 32-40).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize multiple 4 Mb memory planes within the memory array because the system achieve higher system performance by providing multiple memory devices such that read and write or program operations can be performed concurrently (co.1, lines 46-50).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ multiple 4 Mb memory planes for the advantage stated above.

Regarding claim 8, Alexis teaches that the multiple 4 Mb memory planes consist of nonvolatile memory cells (col.1, lines 19-21 and lines 43-45).

Regarding claim 9, Alexis teaches that the nonvolatile memory cell is a flash memory cell (Fig.1 and 2, flash memory 115).

Regarding claim 10, Alexis teaches that the write partition has a dynamic memory address, wherein the memory address changes any time a program or erase operation begins or resumes in a new memory plane (Fig.3, col.7, lines 38 to col.8, lines 15).

Regarding claim 11, Alexis teaches that if no program or erase operation is performed, the read partition and the write partition are allocated to the same memory location (read-while write operation and col.6, lines 52-60).

10. Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexis et al., US Patent 6,182,189 B1, in view of Dalvi et al., U.S 2001/0011318 A1.

Regarding claim 15, Alexis teaches the claimed invention (claim 14), Alexis does not teach the output status bits further comprise: an erase suspend status bit; an erase status bit; a program status bit; a voltage status bit; a program suspend status bit and a

device protect status bit. However, Dalvi teaches that an output status bit comprising an erase suspend status bit (ESS); an erase status bit (ECLBS); a program status bit (WSMS); a voltage status bit (Vpp); a program suspend status bit (col.2, section 0012, first two lines) and a device protect status bit (BWSLBS).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Dalvi in the system of Alexis and use a status register stores multiple memory bits which provides a specific status signal for improving the efficiency of the computer system (col.2, section 0026, last two lines and section 0028, last two lines).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 17, Alexis and Dalvi teach the claimed invention (claim 15), Dalvi further teaches that the program status bit, the erase status bit, the program status suspend bit and the erase status suspend bit are a logical OR of the information of each of the M partitions.(col.1, section 0006, lines 9-17 and col.2, section 0025, lines 3-6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the logical OR for the above status bits which provides a specific status signal, for example, whether a specific operation has been completed successfully or unsuccessfully or in progress, the information stored in the status

register often provides necessary or desirable information to other components in a system (col.1, section 0002), therefore, improving the efficiency of the computer system (col.2, section 0026, last two lines and section 0028, last two lines).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hazen et al., U.S. Patent 6088264

Hoy et al., U.S. Patent 5765017

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7238 for regular communications and 703-746-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

August 22, 2003

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100